MARC4 – 4-bit Microcontroller

The M43C200 is a member of the TEMIC family of 4-bit single chip microcontroller. It contains ROM, RAM, parallel I/O ports and on-chip clock generation.

Features

- **Stack oriented HARVARD architecture**
  – 4K × 8-bit ROM
  – 256 × 4-bit RAM
  – 2 µs instruction cycle
  @ 4 MHz OSC-frequency
- **Programming**
  – User friendly in high level language qForth
- **Development system**
  – PC-based
  – Highly optimising compiler
- **Low power**
  – STOP mode @ 1 µA
  – SLEEP mode typically 500 µA
  – RUN mode typically 3 mA
- **High operating range**
  – Supply voltage range 2.4 to 6.2 V
  – Temperature range –40 to 85°C
- **Interrupt structure**
  – 2 external hardware interrupts
  – 1 prescaler/timer interrupt
  – Software interrupts
  – Autosleep

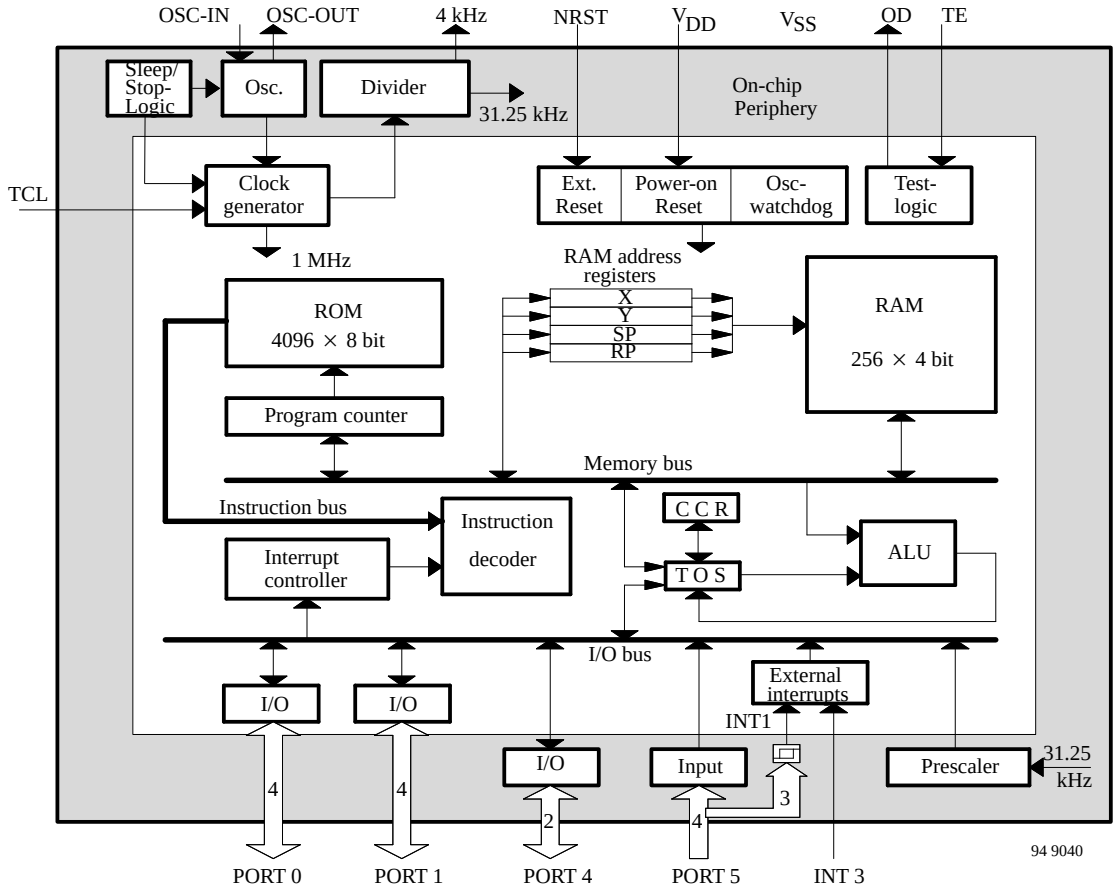


Figure 1. Functional block diagram

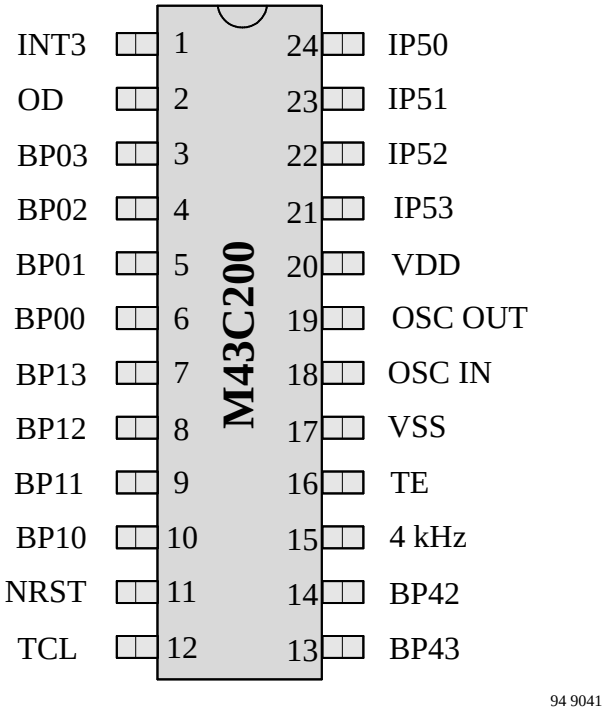


Figure 2. Pin assignment SO24 (top view)

Table 1. Pin description

Pin	Function
V_{DD}	Power supply voltage 2.4 to 6.2 V
V_{SS}	Circuit ground
BP00 – BP03	4 bidirectional I/O lines of port 0 *)
BP10 – BP13	4 bidirectional I/O lines of port 1 *)
BP42 – BP43	2 bidirectional I/O lines of port 4 *)
IP50 – IP53	4 input lines of port 5
OSCIN	Oscillator input (32-kHz crystal)
OSCOUT	Oscillator output (32-kHz crystal)
INT3	External interrupt input
4 kHz	4 kHz output
OD	OD signal for emulation
NRST	Reset input / output, a logic low on this pin resets the device.
TCL	External system clock I/O. This pin can be used for external clock operation.
TE	Testmode input. This input is used to control the test modes and the function of the TCL pin.

*) The I/O ports have CMOS output buffers. As input they are available with pull-up or pull-down resistors. Please see the order information.

Contents

Contents (continued)

1 General Description

The M43C200 is a member of the TEMIC MARC4 family (single chip **M**odular **ARC**hitecture **4-**bit microcomputers). It contains ROM, RAM, I/O-ports, 15 stage prescaler, 4-MHz oscillator and two external interrupts.

Note: For the self-test program about 0.5 Kbyte of the 4 Kbyte ROM are required.

The CPU is built around a stack based Harvard type architecture, where the program memory (in ROM) and the data memory (in RAM) are physically separate and addressed independently.

The M43C200 has a typical instruction cycle time of 2 µs @ 4 MHz oscillator frequency.

The SLEEP instruction allows the CPU to be stopped by the program, thereby enabling reduction in current consumption. Once the CPU has entered SLEEP mode it can be revived into active state immediately, following the receipt of an interrupt. In SLEEP mode, the CPU is held in a defined state whereby all data are latched. In the SLEEP mode the 4-MHz oscillator and the prescaler/ timer are still running. It gives the opportunity to wake up the CPU in a defined time which is given by the prescaler.

The highest power saving mode is the STOP mode. In this case the CPU, oscillator and prescaler are all stopped controlled by the internal NRUN-signal. If an interrupt appears the 4-MHz oscillator will be started, controlled by the SLEEP/ STOP logic. When the oscillator has reached the exact frequency a reset is generated and the program will start the $RESET routine.

1.1 Interrupt Structure

The MARC4 can handle up to eight priority interrupts which can be generated from on-chip modules (prescaler), external sources (interrupt pads) or synchronously from the CPU itself (software interrupts).

An additional power-on reset interrupt is used for initialising the CPU. This reset signal can also be supplied from the RST pad. The purpose of the power-on reset is to start the oscillator and to put the CPU into a well defined condition after the operating voltage has been reached. The reset interrupt has the absolute highest priority having access to the CPU at all times. The processor will automatically enter SLEEP when the lowest priority task has been completed, so making maximum use of the power saving capabilities of the MARC4.

1.2 Prescaler

A programmable prescaler driven by 31.25 kHz offers 1 interrupt. Table 2 (page 14) illustrates the eligible interrupt frequencies. The prescaler powers up in the reset condition.

2 Pin-, Signal-, Memory-, Core Registers- and Self-Check Description

2.1 Pin Description

2.1.1 V_{DD}, V_{SS}

V_{DD} is the power for the µC core, RAM, ROM and the peripherals, V_{SS} is ground.

2.1.2 NRST

The NRST input is not required for start-up but can be used to reset state of the microcontroller and provide an orderly software start-up procedure. Refer to **Reset modes** in section for a detailed description.

2.1.3 TCL

The system clock for the microprocessor is derived from a fully integrated on-chip crystal oscillator circuit. This oscillator tracks the supply and temperature to ensure optimum operation of the microcontroller under all conditions.
The TCL pin is necessary as clock input for the test- and emulation mode.

2.1.4 TE, OD

These two lines are needed for test and emulation.

2.1.5 OSCIN, OSCOUT

An oscillator with a divider stage is integrated in the chip to generate the 1-MHz clock frequency (TCL). This oscillator is operated by simple connection of 4-MHz quartz or ceramic resonator.

This oscillator can be controlled via port 42 (NRUN-signal). This means that the oscillator can be stopped in SLEEP mode or remains active if operation of the prescaler is desired. However, this function can only be set by software.

INRUN – signal “high”
the µC goes in sleep mode after finishing the lowest (Port 42) interrupt (oscillator running)

INRUN – signal “low”
the µC goes in STOP mode after finishing the lowest interrupt (oscillator stop).

2.1.6 Bidirectional Ports

Port 0, 1 and 4 may be programmed as input or output under software control. The direction of a port is determined by an IN or OUT instruction and is held until another IN or OUT instruction for this port is executed.

The direction of this bidirectional ports is not switchable on a bit-wise basis. The output latches hold the state of last data value written to the port. At power-on or external reset all pins of port 0, 1 and 4 are set to input mode and all output latches are set to a logic 1. Whenever the port is switched from input to output the last value stored in the latches will appear on the outputs for one clock cycle.

When switching bidirectional ports from output to input the stray capacitance of the connection wires may cause the data read to be the same as the last data written to this port. This behaviour can be used by connecting large enough capacitors to the pins of the bidirectional port to read back the previous data written to this port. On the other hand, to avoid the negative effects of stray capacitance the following approaches should be used:
Use two IN instructions, and DROP the first data nibble read.

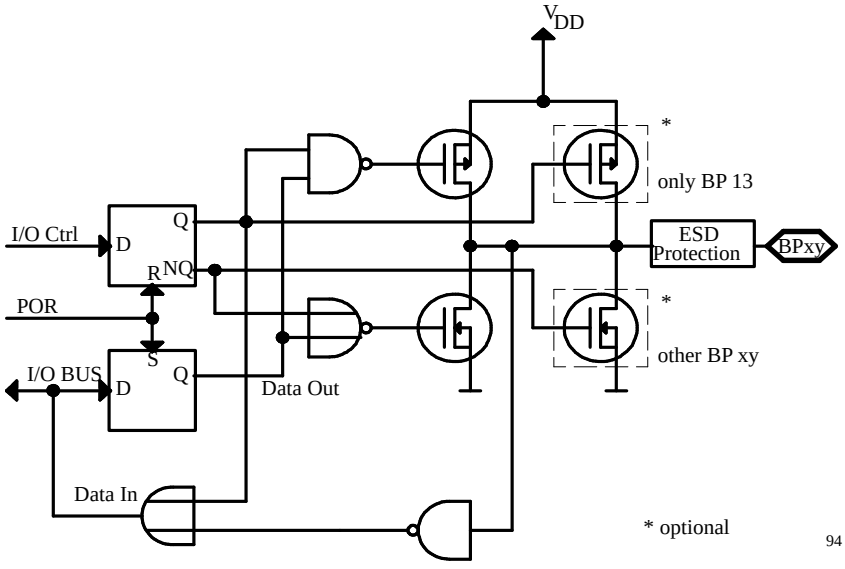
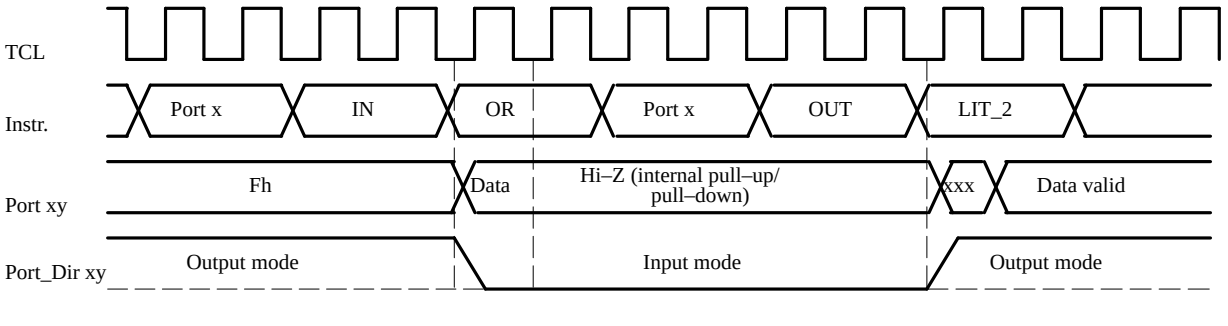


Figure 3. Bidirectional port schematics



xxx) Last written data contained in output latches, Fh after power–on–reset

Figure 4. Read and write cycle timing

2.1.7 Input Port 5

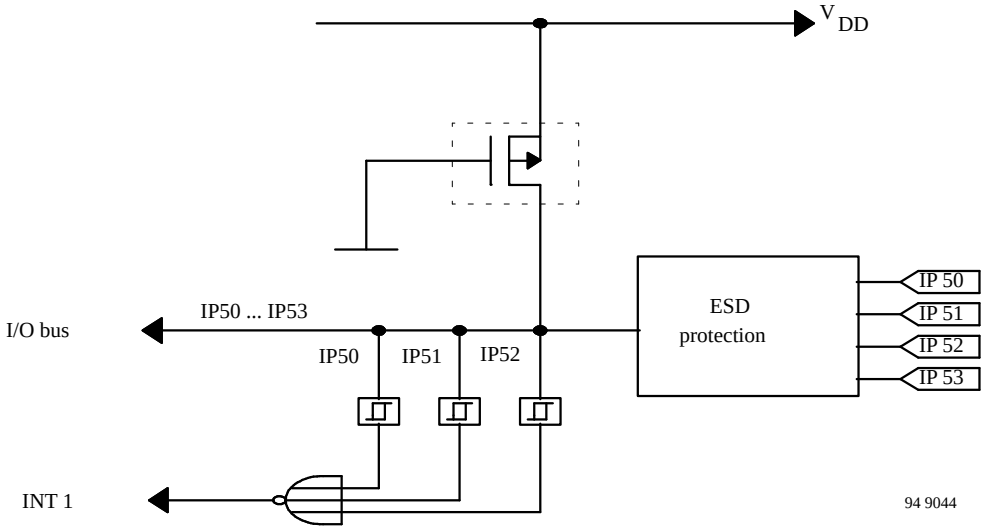


Figure 5. Input port

The data on port 5 is sent to the top of the expression stack whenever an IN instruction (addressing port 5) is executed. The pins IP50, IP51 and IP52 of the port 5 may generate an additional interrupt (priority level 1), when any of the three input lines is driven low. This function is useful for implementing an interrupt driven keyboard. The interrupt lines are negative edge triggered and have Schmitt-trigger characteristics to improve the noise immunity. The interrupt function is enabled after power-on or external reset. This interrupt can be disabled by software.

2.2 Memory

The MARC4 family of microcontroller is based on the Harvard architecture with physically separate program memory (ROM) and data memory (RAM).

The program memory (ROM) is mask programmed with the customer application program during the fabrication of the microcontroller. The ROM is addressed by a 12-bit wide program counter, thus limiting the program size to a maximum of 4096 bytes which cannot be extended by using external memory. The user ROM starts with a 512 byte segment (‘Zero Page’) which contains predefined start addresses for interrupt service routines and special subroutines accessible with single byte (SCALL) instructions. The corresponding memory map is shown in figure 6.

The self test routines should be included as part of the free program space. The 16-bit check sum (CRC) is located by the compiler in the last two bytes of ROM.

The on-chip 256 × 4 bit RAM is divided in the 12-bit wide return stack, the 4-bit wide expression stack (both with a user definable depth) and the data memory. The fixed return address (00h) which points to the $AUTOSLEEP routine is located at RAM address FCh.

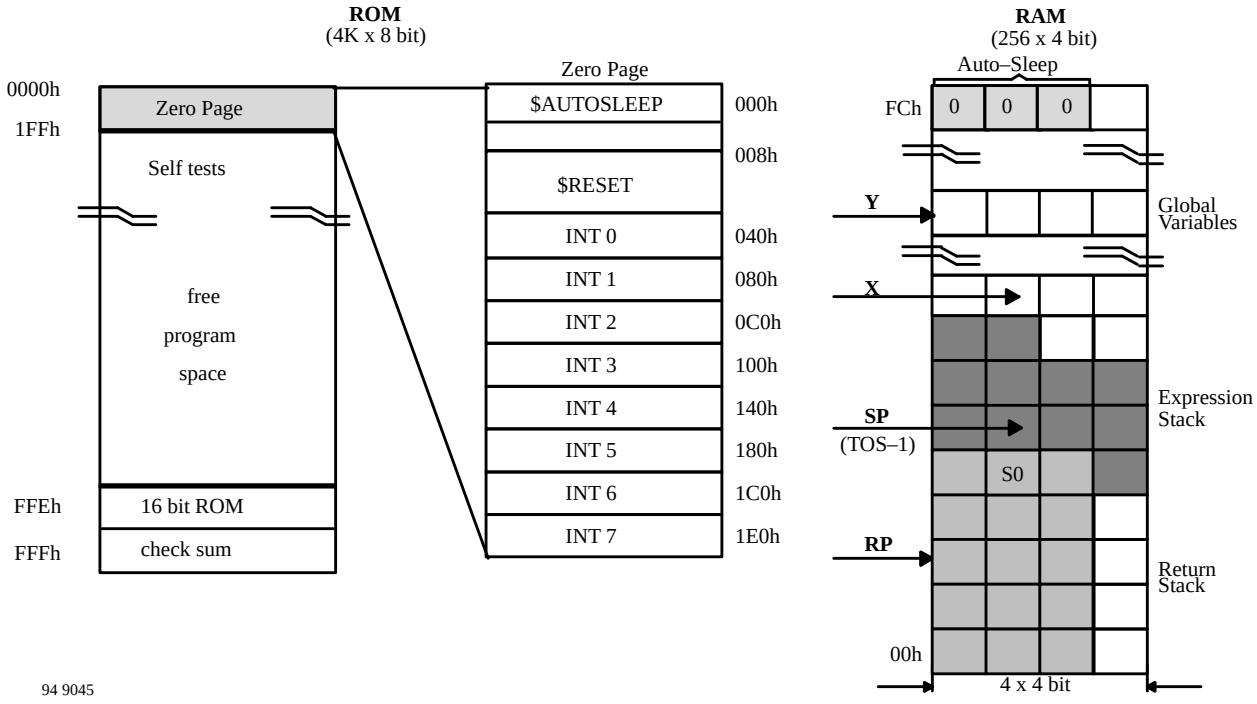


Figure 6. Memory map

2.3 Core Registers

As shown in the programming model below, the MARC4 core has seven registers.

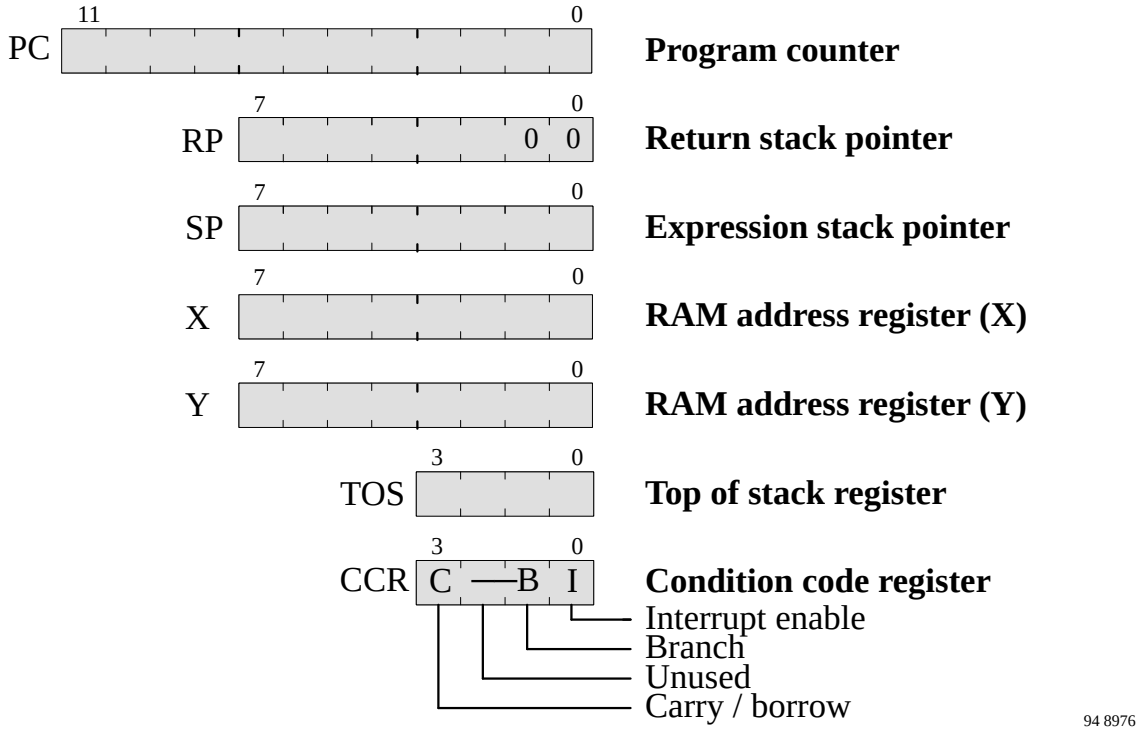


Figure 7. Programming model

2.3.1 Accumulator (TOS)

Because this microcontroller is a stack based machine with two on-chip stacks located in the internal RAM, all arithmetic, I/O and memory reference operations take their operands from, and return their results to the 4-bit wide expression stack. This stack is also used for passing parameters between subroutines, and as a scratchpad area for temporary storage of data. The top element of the expression stack is immediately accessible through the TOS register. The MARC4 can perform most of the operations dealing with the top of stack items (TOS and TOS-1) in a single byte, single cycle instruction.

2.3.2 Expression Stack Pointer (SP)

The 8-bit wide stack pointer SP contains the address of the next-to-top 4-bit item (TOS-1) on the expression stack, located in internal RAM. After power-on reset the stack pointer has to be initialised to the start address of the allocated expression stack area (S0).

2.3.3 RAM Address Register (X and Y)

The 8-bit wide register X and Y are used to address any 4-bit item in the RAM.

Using either the pre-increment address mode it is comfortable to compare, fill or move arrays in the RAM area.

2.3.4 Return Stack Pointer (RP)

The return stack pointer (RP) points to the top element of the return stack.

The 12-bit return stack is used for storing subroutine return addresses and keeping loop index counts. The return stack can also be used as a temporary storage area. The MARC4 instruction set supports the exchange of data between the top elements of the expression and return stack. The return stack automatically pre-increments and post-decrements in steps of 4. This means that every time a subroutine return address is stacked, 4-bit RAM locations are left unwritten. This locations are used by the qFORTH compiler to allocate 4-bit variables.

After power-on reset the return stack pointer has to be initialised to FCh.

2.3.5 Program Counter (PC)

The program counter (PC) is a 12-bit register that contains the address of the next instruction to be executed by the microcontroller.

2.3.6 Condition Code Register (CCR)

The 4-bit wide condition code register (CCR) indicates the results of instruction just executed as well as the state of the microcontroller. These bits can be individually tested by a program and specified action will take place as a result of their state. Each bit is explained in the following paragraphs.

Carry/Borrow (C)

This flag indicates that a borrow or carry out of the arithmetic logic unit (ALU) occurred during the last arithmetic operation. This bit is also affected during shift and rotate operations and the execution of SET_BCF, CLR_BCF and CCR! instructions.

Zero (Z)

When the bit is set, it indicates that the result of the last arithmetic or logical manipulation was zero.

Branch (B)

A conditional branch takes place when the branch flag was set by one of the previous instructions (e.g., a comparison operation).

Instructions such as SET_BCF, TOG_BF and CLR_BCF allow the direct manipulation of the branch flag under program control. The flag is affected by all ALU operations except CCR@, DI, SWI, RTI and OUT.

Interrupt Enable (I)

This flag is used to interrupt processing on global basis. Resetting the interrupt enable flag (using the DI instruction) disables all interrupts. The µC does not process further interrupt requests until the interrupt enable flag is set again by either executing an EI, RTI (return-from-interrupt) instruction or entering the SLEEP mode. After power-on or an external reset the interrupt enable flag is automatically reset. The RTI instruction at the end of the $RESET routine will set the interrupt enable flag and thereby enable all interrupts.

2.3.7 Self-Check

The self test capability of the MARC4 provides the possibility of checking the core, ROM, RAM, interrupt and prescaler easily. The $RESET routine (after power-on reset) allows to choose the test routine or the application program.

Note: The necessary test routine were delivered by TEMIC.

3 Reset Modes, Interrupts, Prescaler and Low Power Modes

3.1 Reset Modes

The M43C200 has three reset modes: an active low external reset pin (RST), a power-on and an oscillator watchdog reset function.

3.1.1 External Reset (NRST)

The external reset (NRST) input pin is used to provide an orderly software startup procedure of the µC. When using the external reset mode, the RST pin should be low for a minimum of two instruction cycle times (typically 4 µs). The pin RST has an internal pull-up.

3.1.2 Power-on Reset

The power-on reset occurs when a positive transition is detected on the power supply input. The power-on reset is used strictly for power turn-on conditions and should not be used to detect any drops in the power supply voltage. A power-down reset occurs when a negative transition is detected on the power supply input for 5 ms or more. To improve noise immunity the power-on reset has Schmitt-trigger characteristics as shown in figure 8.

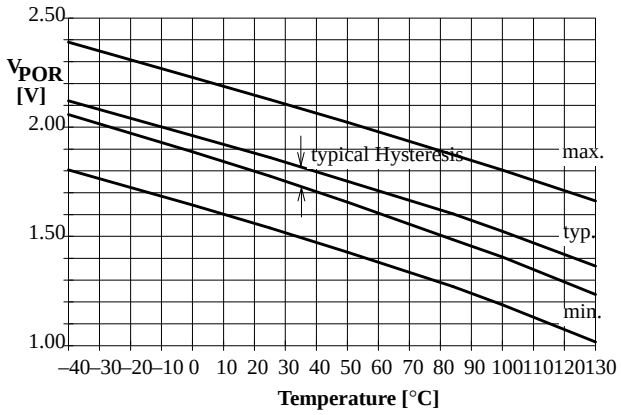


Figure 8. Temperature versus V_{POR}

3.1.3 Oscillator – Watchdog Reset Function

The oscillator-watchdog guarantee a well-defined clock condition by using a quartz or a ceramic resonator.

After starting, normally this sorts of oscillator generates undefined clock signals. In this case the amplitude is controlled by the oscillator-watchdog. When the right value of oscillator-amplitude is detected the RST-pin will be hold LOW for 32 oscillator periods. After this time the µC starts the $RESET routine.

When extern clock is used (pin OSCOUT as clock input) the amplitude must be $0.9 \times V_{DD}$ otherwise the oscillator watchdog will detect an error.

3.1.4 Effects on Internal Circuitry

All reset modes guarantee a well-defined start condition of the complete microcontroller. During RESET all interrupts are disabled, all pending and active interrupts are cleared, all on-chip peripherals are reset and a non-maskable interrupt request is generated. The RESET has the absolute highest priority, having access to the microcontroller at all times.

	Function	Located in ROM at	Max. Length [ROM bytes]	Interrupt Opcode
$RESET	Software & hardware initialization	008 h	56	C1 h

The main tasks of the reset service routine ($RESET) are:

- Stack pointer initialization,
- Variable and array initialization, and
- Initialisation and setup of the peripherals.

After execution of the reset service routine, the interrupts are enabled automatically by the RTI or previously executed EI instruction.

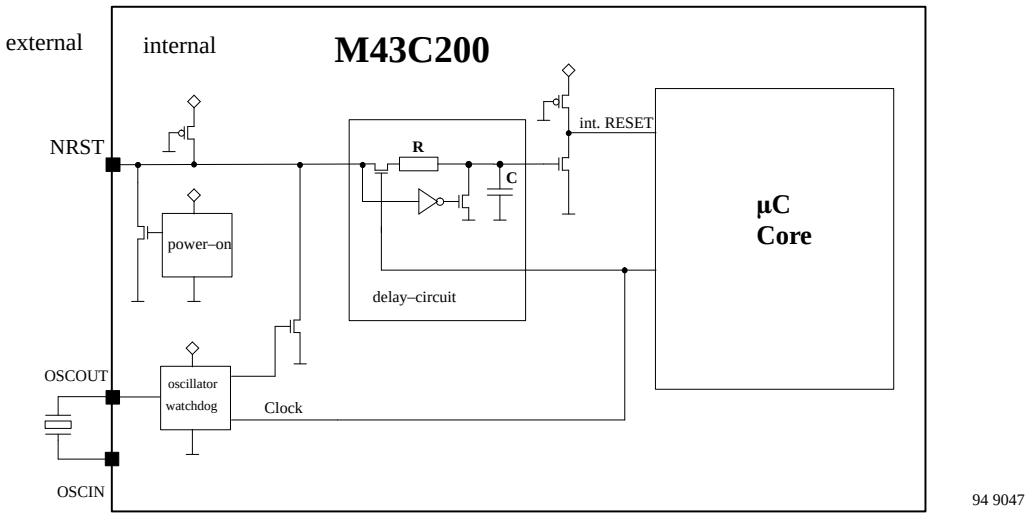


Figure 9. Reset functions

3.1.5 Summary of all Reset Functions

Figure 9 shows all reset functions: external NRST, power-on and oscillator-watchdog. All these resets will generate an internal reset after passing the delay circuit. Normally the delay time is about 40 periods of the system frequency (TCL).

3.2 Interrupts

The M43C200 can handle interrupts of 8 priority levels (table 1). They are generated from on-chip modules (prescaler), external sources (port 5 and interrupt pad) or synchronously from the core itself (software interrupts). Each interrupt source has a hard-wired interrupt priority and an associated interrupt service routine in the program ROM. The programmer can enable or disable all interrupts by setting or resetting the interrupt enable flag in the CCR using the EI or DI instruction.

When the interrupt enable flag is reset (interrupts disabled), the execution of interrupts is inhibited but not the logging of the interrupt requests in the interrupt pending register. While interrupts are disabled (e.g., for a time critical section of code) and an interrupt is generated the interrupt will not be lost. Its execution will only be delayed until interrupts are enabled again. Interrupts are only lost when the pending register for a particular interrupt priority is still set at the time of a further interrupt transmission of the same level. The pending resister is reset either on power-on reset or on compilation of corresponding interrupt service routine by execution the RTI instruction (see figures 10 and 11).

The µC automatically enters the SLEEP mode when the lowest priority interrupt service routine has been completed. This guarantees a maximum use of the power saving capabilities of the µC. For further information please refer to low power modes.

Table 1. Interrupt priority and address allocation map

Priority	Function	Located in ROM at	Max. Length [ROM bytes]	Interrupt Opcode
INT7	Software interrupt	1E0h	> 24	**FCh**
INT6	Software interrupt	1C0h	32	**F8h**
INT5	Software interrupt	180h	64	**F0h**
INT4	Prescaler interrupt	140h	64	**E8h**
INT3	External hardware interrupt negative edge triggered	100h	64	**E0h**
INT2	Software interrupt	0C0h	64	**D8h**
INT1	External hardware interrupt negative edge triggered (port 50, 51, 52)	080h	64	**D0h**
INT0	Software interrupt	040h	64	**C8h**

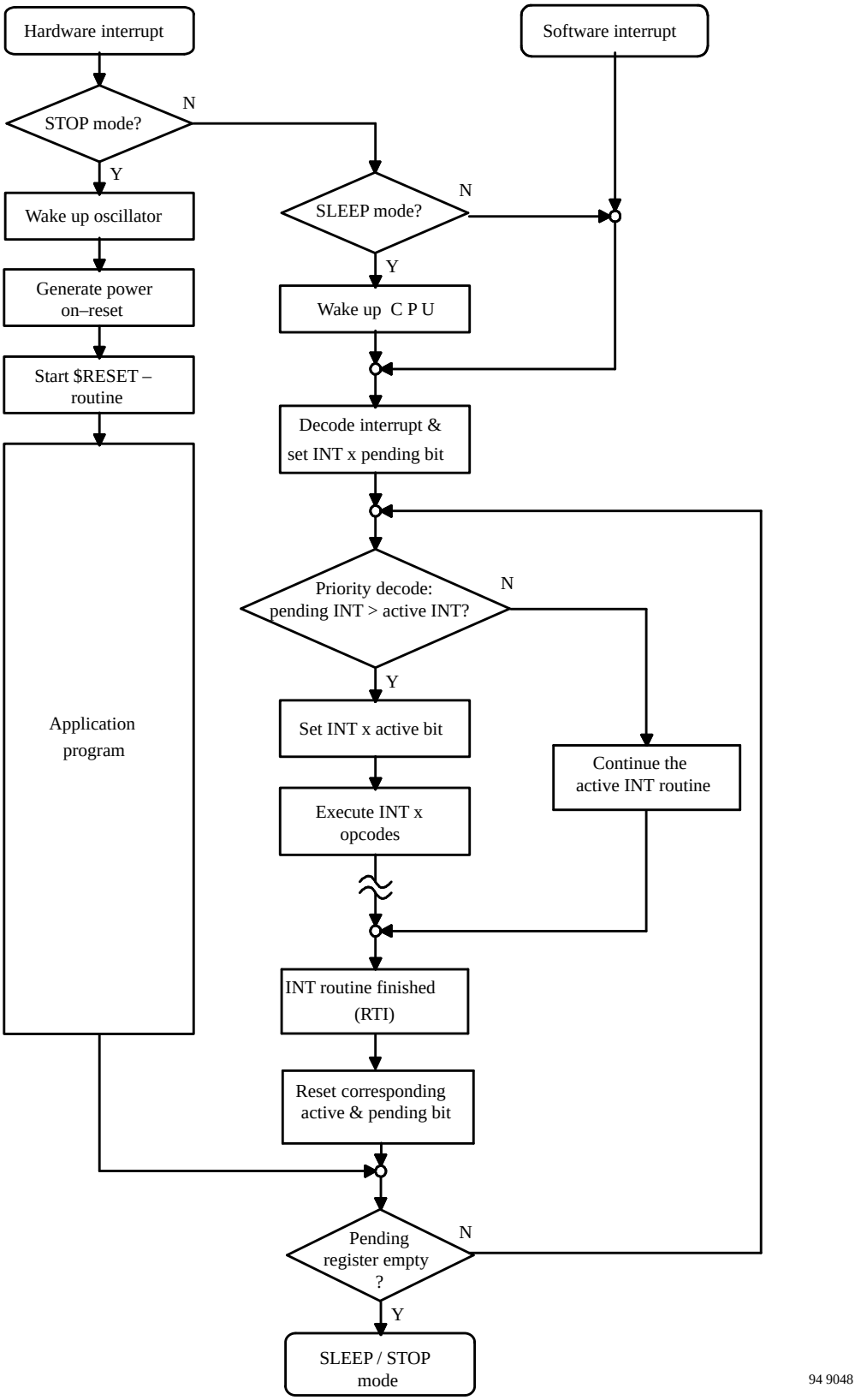


Figure 10. Interrupt flow chart

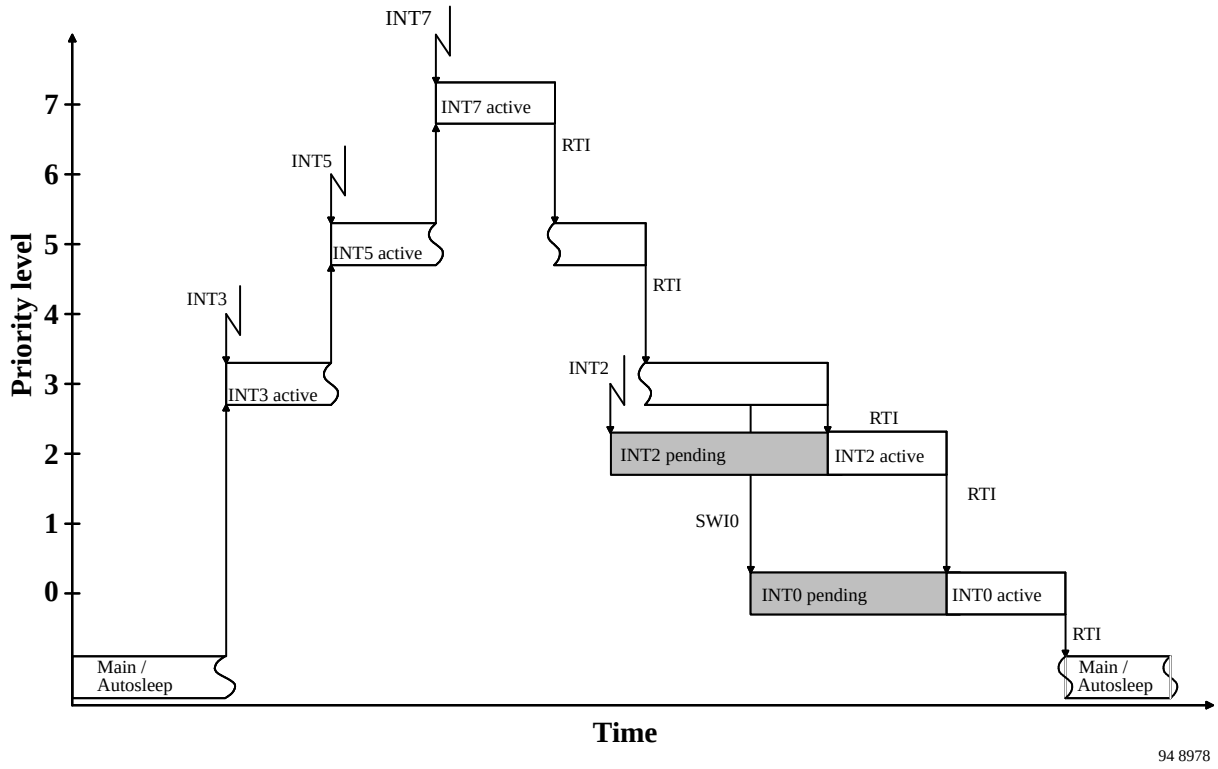


Figure 11. Interrupt handling

3.2.1 Interrupt Handling

The integrated interrupt controller samples all interrupt requests and latches these in the interrupt pending register. It also decodes the priority of the interrupt requests, and signals the µC when a higher priority interrupt requests is present. If the µC (with interrupts enabled) receives the interrupt controller's signal, an interrupt acknowledge cycle will be entered. During this cycle, the µC saves the current PC on the return stack and loads the PC with the start address of the corresponding interrupt service routine. When the µC is in the SLEEP mode, it will be activated by any hardware interrupt, by the means of wake-up the CPU and decoding the interrupt.

Using the MARC4 way of interrupt transmission, it is possible to transmit more than one interrupt at the same time. The transmitted interrupts are loaded into the interrupt pending register asynchronously. The priority decoder determines the interrupt with the highest priority and activates it as shown in figure 11.

If the µC was in stop-mode any interrupt will start the oscillator. This will generate a reset and starts the $RESET routine.

3.2.2 Interrupt Latency

The interrupt latency is the time from the falling edge of the interrupt to the interrupt service routine being activated. This time is between three or five instruction cycles depending on the state of the core. The highest frequency which can be reasonably handled on the duty cycle of the application.

3.2.3 Software Interrupts

Software interrupts are executable instructions which are supported by predefined macros named SWI 0 through SWI 7. The software triggered interrupts operates exactly like any hardware triggered interrupt.

3.2.4 Hardware Interrupts

Port 5 interrupt

Any of the input port 50, 51 and 52 may generate an interrupt level 1 (see figure 5). The INT1 is negative edge triggered and has Schmitt-trigger characteristics.

External interrupt

The external interrupt INT3 is negative edge triggered and has Schmitt-trigger characteristics to improve the noise immunity (see figure 12).

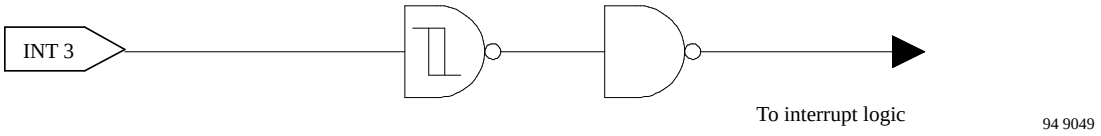


Figure 12. External interrupt input

3.3 Prescaler Interrupt

The programmable prescaler is usually driven by an internal frequency of 31.25 kHz. The prescaler consists of a stage divider chain. This divider chain offers an interrupt source with the priority level 4. The prescaler module powers up in the reset condition which corresponds to control code Fh. The prescaler interrupt (INT4) has 15 programmable taps from 15.625 kHz down to 1 Hz. They are selectable by writing a value of E...0 into the control register at port address 15.

3.3.1 Prescaler During SLEEP Mode

When the microcontroller enters the SLEEP mode, the core clocks are halted. While the 4 MHz oscillator and prescaler remain active, all µC actions are suspended. The microcontroller exists in the SLEEP mode when an interrupt is generated by the prescaler (in addition to a logic low on an external interrupt (INT3), port 50, 51, 52 input pin (INT1), or an external reset).

3.4 Low Power Modes

Two low power consumption modes of operation are available: SLEEP and STOP mode. These operating modes are initiated by executing the SLEEP instruction.

Note: The SLEEP instruction is not a normal instruction as its function is depended on the state of the interrupt pending register. SLEEP is therefore available for use within the $AUTOSLEEP routine only.

3.4.1 SLEEP Mode

By executing the SLEEP instruction (in the $AUTOSLEEP routine) the microcontroller enters a low power consumption mode. In this SLEEP mode, the programmable prescaler remains active, while the internal µC clock is turned off causing all core processing to be stopped. It can only be kept when none of the interrupt pending or active register bits are set.

Table 2. Selectable interval times for the prescaler

Control Code Port Address 15	Interrupt Frequency f_C / n	f_C = 31.25 kHz Time Interval
F		reset & hold complete prescaler
E	$n = 2^1$	64 µs
D	$n = 2^2$	128 µs
C	$n = 2^3$	256 µs
B	$n = 2^4$	512 µs
A	$n = 2^5$	1.024 ms
9	$n = 2^6$	2.048 ms
8	$n = 2^7$	4.096 ms
7	$n = 2^8$	8.192 ms
6	$n = 2^9$	16.384 ms
5	$n = 2^{10}$	32.769 ms
4	$n = 2^{11}$	65.536 ms
3	$n = 2^{12}$	131.072 ms
2	$n = 2^{13}$	262.144 ms
1	$n = 2^{14}$	524.288 ms
0	$n = 2^{15}$	1.048 s

During the SLEEP mode, the I bit in the condition code register (CCR) is set to enable all interrupts. All other registers, memory, and parallel input/output lines remain the same. The 4 MHz oscillator is not switched off, but the prescaler may be disabled by the application program. This mode will continue until any interrupt or reset is sensed. At this time the event is decoded and the program counter is loaded with the corresponding starting address of the interrupt or reset service routine.

The MARC4 unique AUTOSLEEP feature allows the µC to enter the SLEEP mode automatically when the lowest priority interrupt service routine has been completed.

The SLEEP mode is a shutdown condition which is used to reduce the average system power consumption in applications where the µC is not fully utilised (figure 13). Using SLEEP and interrupts, the full computational speed of the core is always available. In this way, power is only consumed when needed, allowing the µC to run in high speed bursts from a weak supply (battery, capacitor, or even a solar cell).

Calculating the average power consumption

The total power consumption is directly proportional to the active time of the µC. For a rough estimation of the expected average system current consumption, the following formula should be used:

$$I_{SYS} = I_{SLE} + (I_{DD} * T_{active}/T_{total})$$

3.4.2 STOP Mode

The lowest power consumption mode of the microcontroller is entered with the STOP operation. The current consumption of the µC (without external loads) will be reduced to 1 µA.

The STOP mode can be implemented by switching off power supply of 4 MHz oscillator. This can be done with a combination of INRUN (BP42 “L”) and SLEEP.

During the STOP mode, the I bit in the CCR is set to enable external interrupts. All other registers, memory, and all I/O lines remain unchanged. This continues until an external interrupt or reset is decoded. After an external interrupt or reset the 4 MHz oscillator starts and generates a reset signal. The program counter is loaded with the reset service routine.

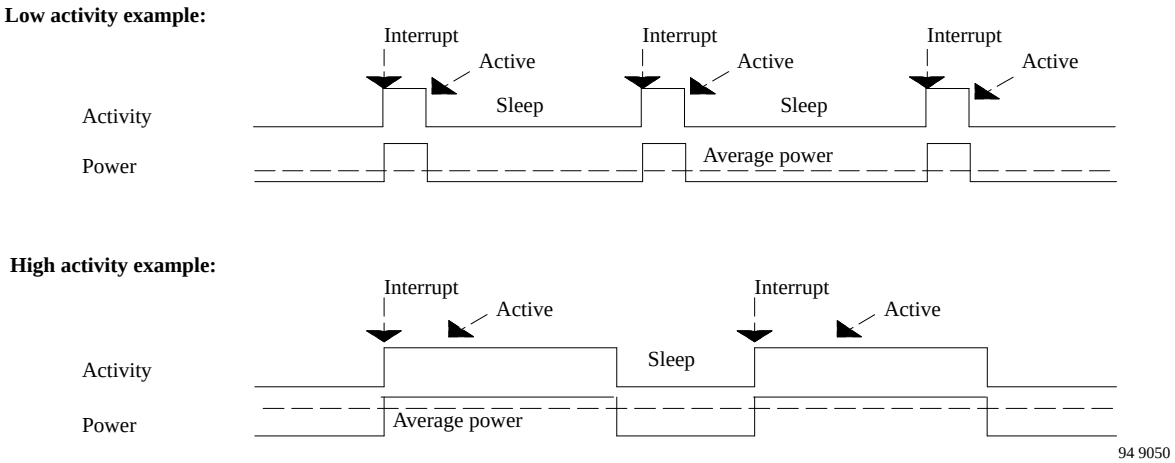


Figure 13. Average system power consumption and duty cycle

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

All voltage are given to V_{SS}.
The circuit is protected against supply voltage reversal for 5 minutes typically @I_{max} = 100 mA.

Parameters	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +7.0	V
Input voltage (on any pin)	V_{IN}	V_{SS} –0.3 ≤ V_{IN} ≤ V_{DD} +0.3	V
Output short circuit duration	t_{short}	indefinite	s
Operating temperature range	T_{amb}	–40 to +85	°C
Storage temperature range	T_{stg}	–40 to +130	°C
Thermal resistance (PLCC)	R_{thJA}	110	K/W
Soldering temperature (t ≤ 10 s)	T_{sd}	260	°C

Absolute maximum ratings define parameter limits which, if exceeded, may permanently change or damage the device is required. All inputs and outputs are highly protected against electrostatic discharges. However, precautions to minimize the built-up of electrostatic charges during handling.

For proper operation it is recommended that V_{IN} and V_{OUT} be limited to the range:

$$V_{SS} < (V_{IN} \text{ or } V_{OUT}) < V_{DD}$$

If in the applications pin 1 (INT3) is not used it must be connected to V_{DD}.

4.2 DC Operating Characteristics

Supply voltage V_{DD} = 2.4 to 6.2 V, V_{SS} = 0 V, T_{amb} = +25°C unless otherwise specified

4.2.1 Supply Currents

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply current active mode	V_{DD} = 2.4 V V_{DD} = 6.2 V	I_{DD}		0.5 2.7	0.7 3.2	mA mA
Supply current SLEEP mode	V_{DD} = 2.4 V V_{DD} = 6.2 V	I_{SLE}		100 600	130 750	µA µA
Supply current STOP mode	V_{DD} = 2.4 V V_{DD} = 6.2 V	I_{STP}		0.08 0.5	0.5 0.8	µA µA

Input voltage pad OD, NRST, TE, port 0, 1, 4, 5

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Input voltage LOW	V_{DD} = 2.4 – 6.2 V	V_{IL}	V_{SS}		0.2 × V_{DD}	V
Input voltage HIGH	V_{DD} = 2.4 – 6.2 V	V_{IH}	0.8 × V_{DD}		V_{DD}	V

4.2.2 Power-on Reset (POR)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
POR voltage		V_{POR}	1.5		2.13	V
POR voltage hysteresis		V_{POR}		100		mV

4.2.3 DC Electrical Characteristics, V_{DD} = 2.4 V @ 25°C

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Pad OD, NRST						
Input current p-channel pull-up	$V_{IL} = V_{SS}$	I_{IL}	–0.8		–5.3	µA
Pad TE						
Input current n-channel pull-down	$V_{IH} = V_{DD}$	I_{IH}	1.1		5.0	µA
Bidirectional ports 0.0 – 0.3, 1.0 – 1.2, 4.2 and 4.3						
Input current n-channel pull-down	$V_{IH} = V_{DD}$	I_{IH}	1.1		5.0	µA
Output current n-channel pull-down	$V_{OL} = V_{SS}$ +0.5 V	I_{OL}	0.7		2.6	mA
Output current p-channel pull-up	$V_{OH} = V_{DD}$ –0.5 V	I_{OH}	–0.6		–2.0	mA
Bidirectional port 1.3						
Input current p-channel pull-up	$V_{IL} = V_{SS}$	I_{IL}	–0.8		–5.3	µA
Output current n-channel pull-down	$V_{OL} = V_{SS}$ +0.5 V	I_{OL}	0.7		2.6	mA
Output current p-channel pull-up	$V_{OH} = V_{DD}$ –0.5 V	I_{OH}	–0.6		–2.0	mA
Input port 5.0 – 5.3						
Input current p-channel pull-up	$V_{IL} = V_{SS}$	I_{IL}	–6.1		–38.2	µA

4.2.4 DC Electrical Characteristics, V_{DD} = 6.2 V @ 25°C

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Pad OD, NRST						
Input current p-channel pull-up	$V_{IL} = V_{SS}$	I_{IL}	–8.0		–51.0	µA
Pad TE						
Input current n-channel pull-down	$V_{IH} = V_{DD}$	I_{IH}	8.2		36.2	µA
Bidirectional ports 0.0 – 0.3, 1.0 – 1.2, 4.2 and 4.3						
Input current n-channel pull-down	$V_{IH} = V_{DD}$	I_{IH}	8.2		36.2	µA

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Output current n-channel pull-down	$V_{OL} = V_{SS} + 1.3$ V	I_{OL}	5.0		13.0	mA
Output current p-channel pull-up	$V_{OH} = V_{DD} - 1.3$ V	I_{OH}	–5.0		–14.0	mA
Bidirectional port 1.3						
Input current p-channel pull-up	$V_{IL} = V_{SS}$	I_{IL}	–8.0		–51	µA
Output current n-channel pull-down	$V_{OL} = V_{SS} + 1.3$ V	I_{OL}	5.0		13.0	mA
Output current p-channel pull-up	$V_{OH} = V_{DD} - 1.3$ V	I_{OH}	–5.0		–14.0	mA
Input port 5.0 – 5.3						
Input current p-channel pull-up	$V_{IL} = V_{SS}$	I_{IL}	–58		–366	µA

4.2.5 Oscillator

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Frequency	C_L = 1 pF	f		4.0		MHz
Integrated input capacitance		C_{IN}		10		pF
Integrated output capacitance		C_{OUT}		10		pF
Start-up time quartz	V_{DD} = 2.4 V *)	t_{SQ}		8	90	ms
	V_{DD} = 3.0 V *)			4.5	10	ms
	V_{DD} = 5.0 V *)			2.5	4	ms
Start-up time ceramic	V_{DD} = 2.4 V **)	t_{SC}		250	—	µs
	V_{DD} = 3.0 V **)			150	300	µs
	V_{DD} = 5.0 V **)			150	160	µs

*) Measured with a typical quartz
C_1 = 3.2 fF
L_1 = 490 mH
R_1 = 40
C_0 = 1.4 pF

**) Ceramic
C_1 = 4.4 pF
L_1 = 385 µH
R_1 = 8.2
C_0 = 36.3 pF

4.3 I/O Port Characteristics

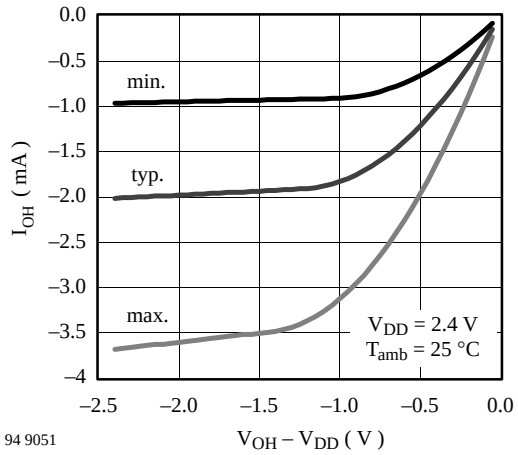


Figure 14. P-channel source current

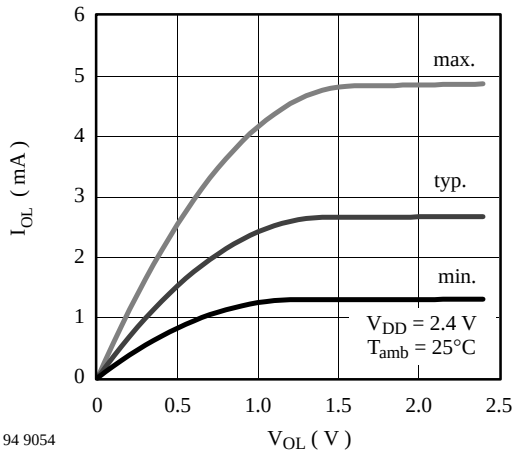


Figure 17. N-channel sink current

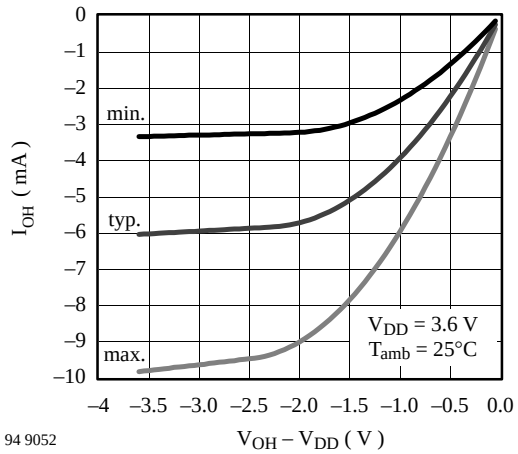


Figure 15. P-channel source current

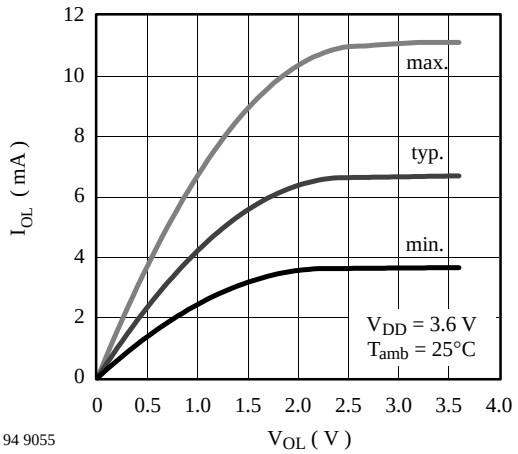


Figure 18. N-channel sink current

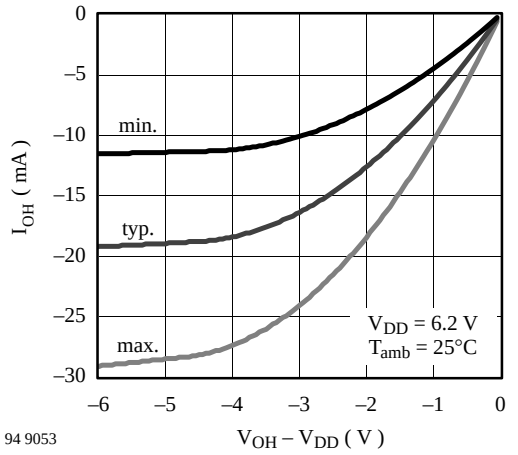


Figure 16. P-channel source current

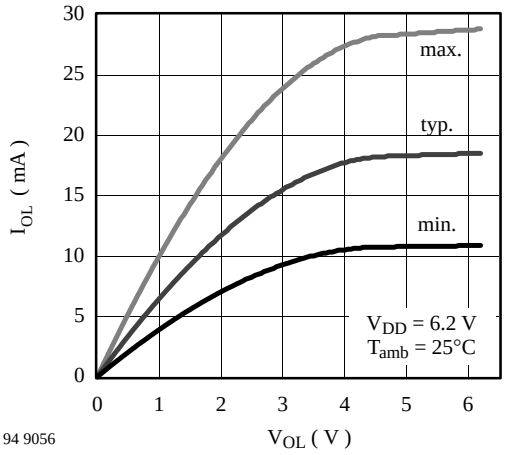


Figure 19. N-channel sink current

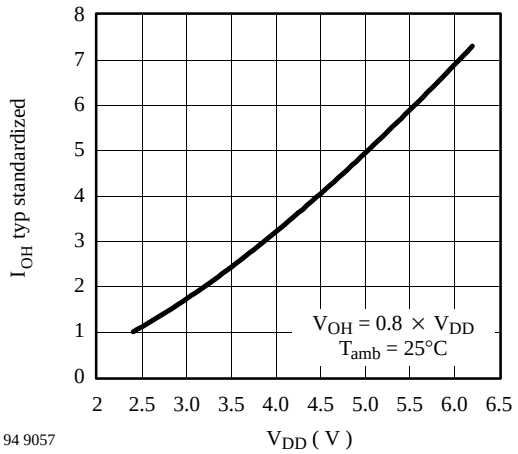


Figure 20. Standardized p-channel source vs. V_{DD}

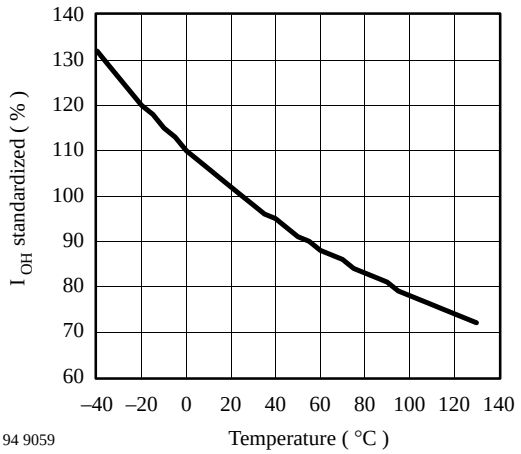


Figure 22. Standardized p-channel source current vs. ambient temperature

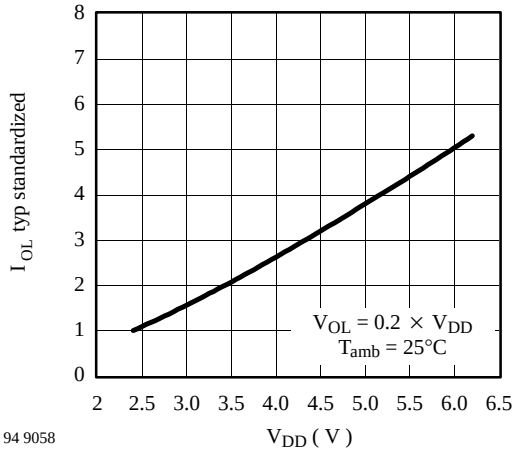


Figure 21. Standardized n-channel sink current vs. V_{DD}

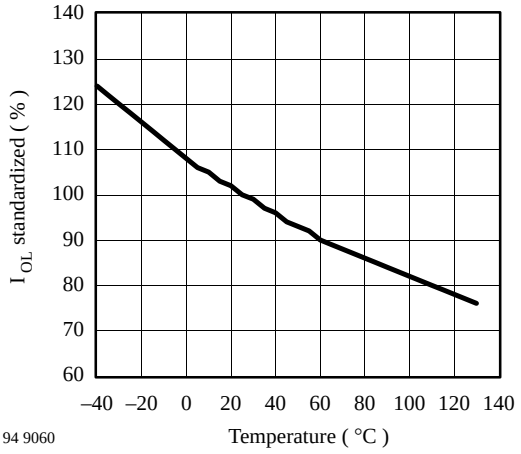


Figure 23. Standardized n-channel sink current vs. ambient temperature

4.4 Characteristics of the Pull-Up and Pull-Down Transistors

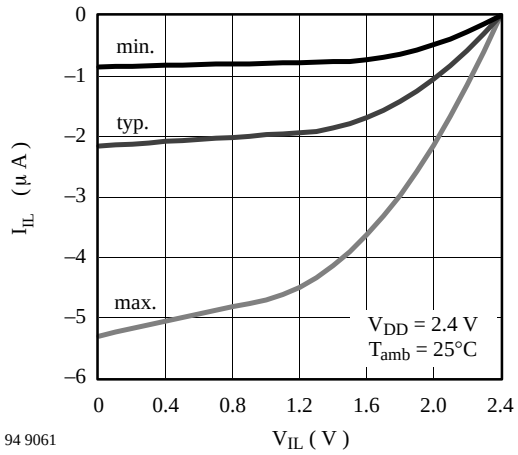


Figure 24. PIN OD: p-channel source current

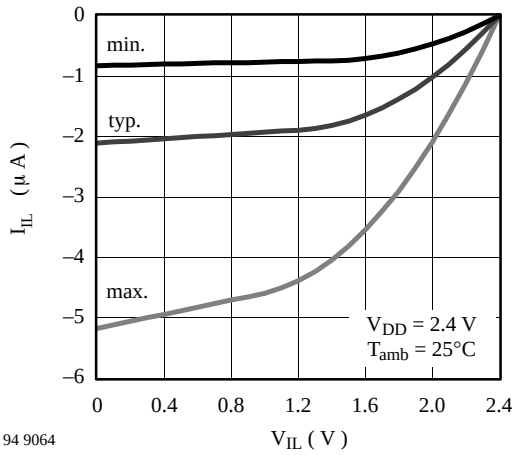


Figure 27. PIN NRST: p-channel source current

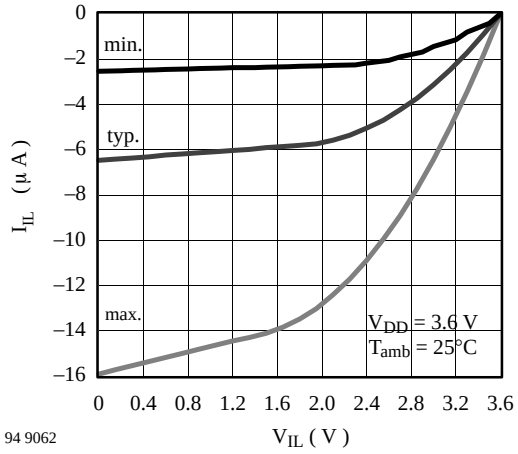


Figure 25. PIN OD: p-channel source current

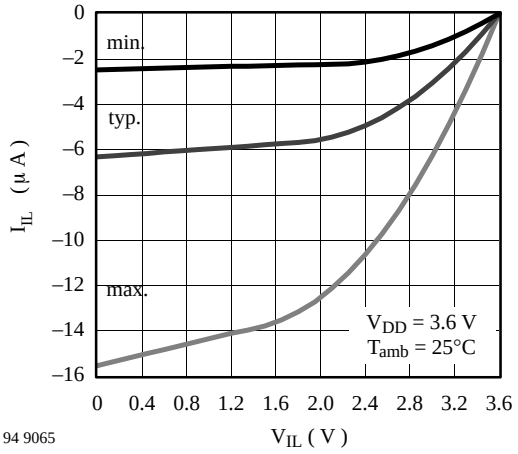


Figure 28. PIN NRST: p-channel source current

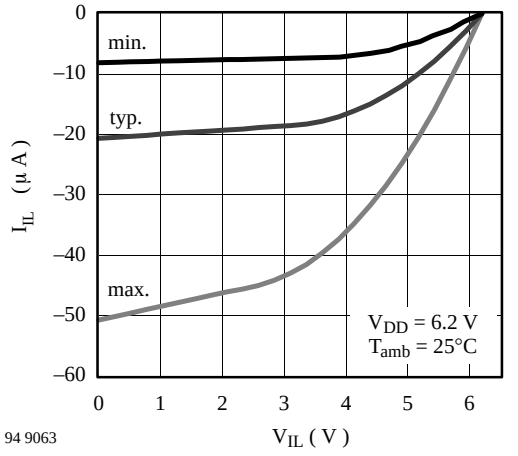


Figure 26. PIN OD: p-channel source current

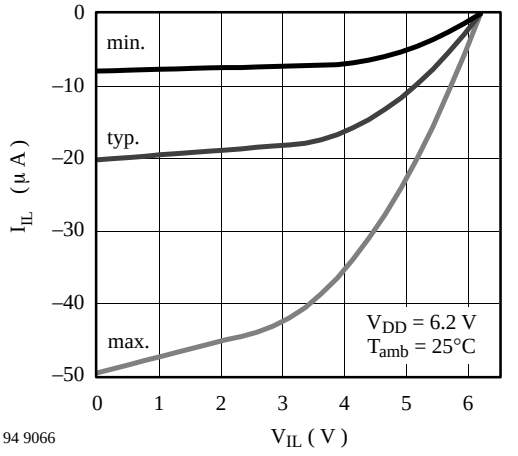


Figure 29. PIN NRST: p-channel source current

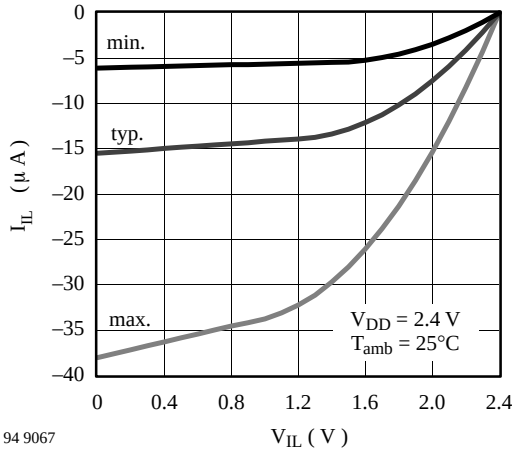


Figure 30. PIN IP5x: p-channel source current

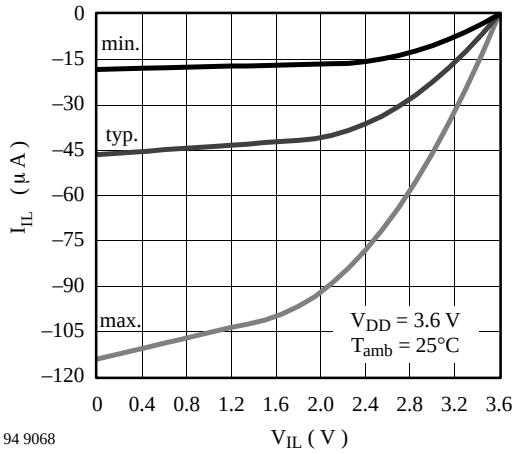


Figure 31. PIN IP5x: p-channel source current

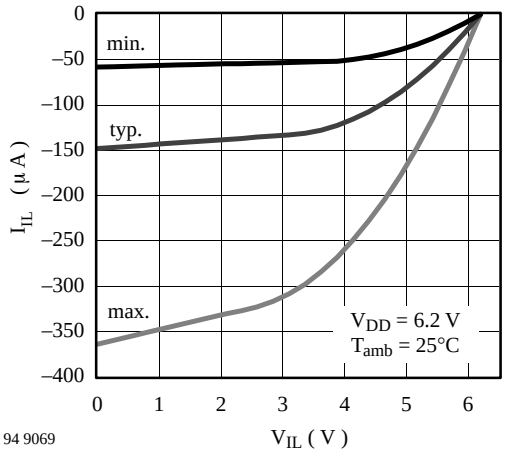


Figure 32. PIN IP5x: p-channel source current

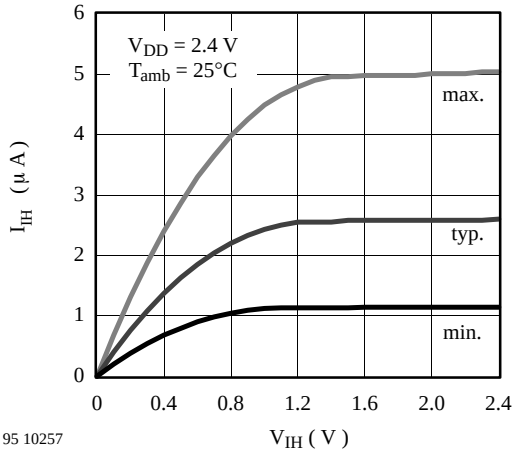


Figure 33. All PINs with pull-down: n-channel sink current

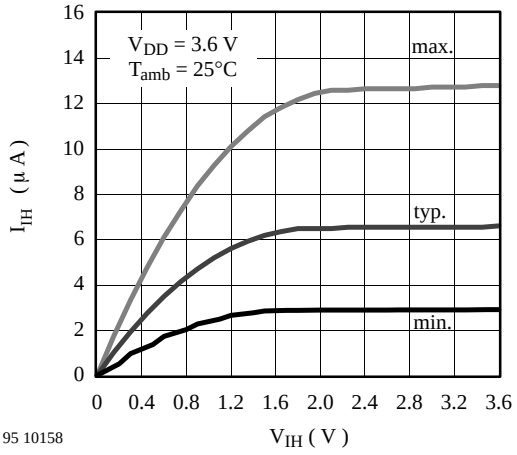


Figure 34. All PINs with pull-down: n-channel sink current

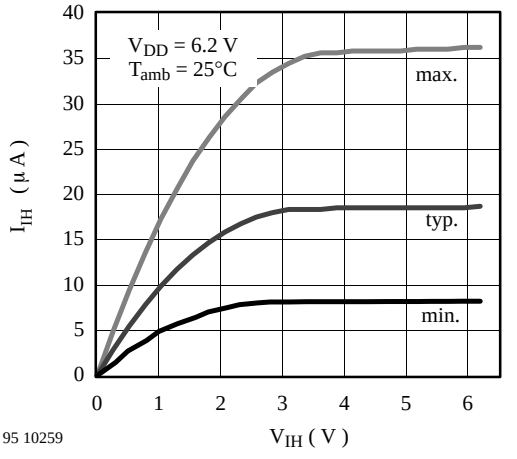


Figure 35. All PINs with pull-down: n-channel sink current

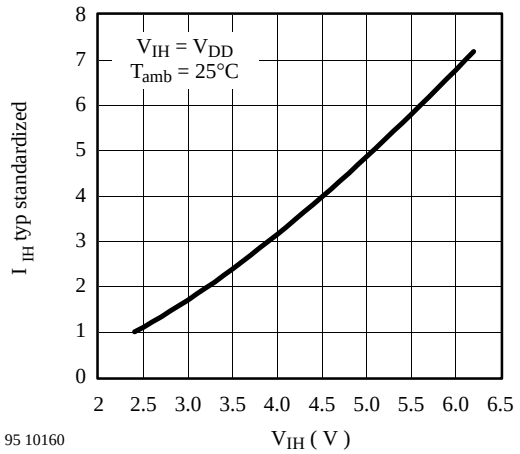


Figure 36. Standardized p-channel source current vs. V_{DD}

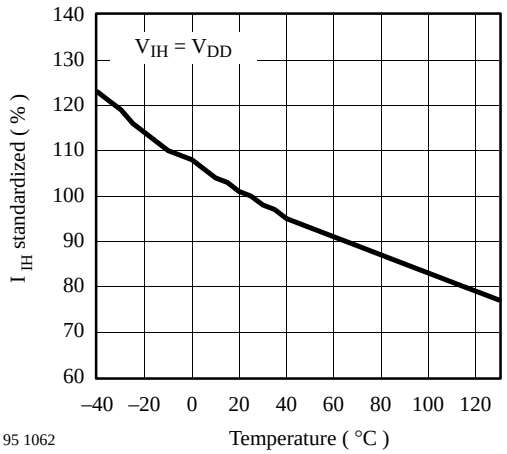


Figure 38. Standardized p-channel source current vs. ambient temperature

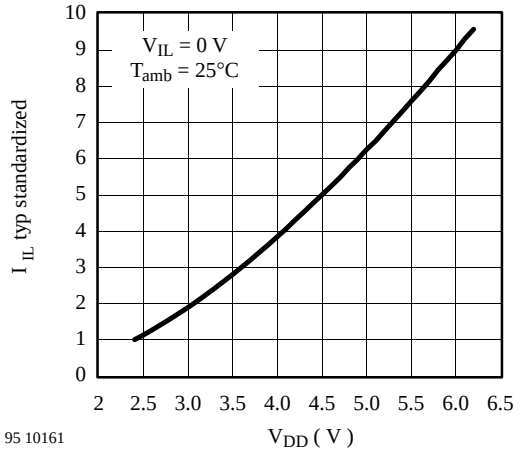


Figure 37. Standardized n-channel sink current vs. V_{DD}

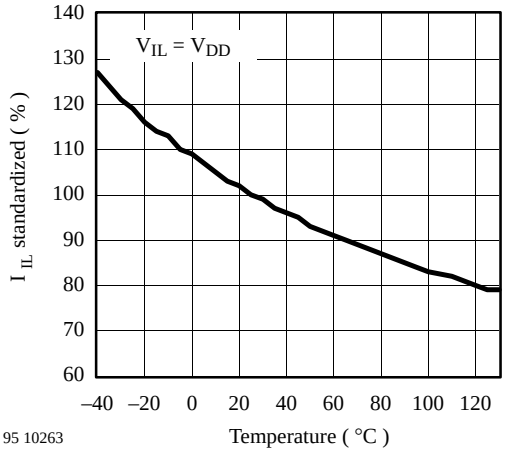
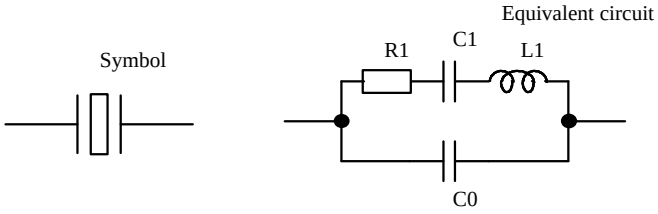


Figure 39. Standardized n-channel sink current vs. ambient temperature

5 Characteristics of the On-Chip Quartz / Ceramic Oscillator

Equivalent Circuit of the Quartz and Ceramic Resonator



The criteria for oscillation depends on R1 and C0. Following diagrams show the equivalent quartz circuits over temperature range –40 to +125°C for two different values of V_{DD}. The figure below shows the maximal values of the equivalent circuit of the ceramic-resonator for start up at V_{DD} = 3.0 V and ambient temperature range from –40 to +125°C. For this test a resonator CSAC4.00 (MURATA) was used.

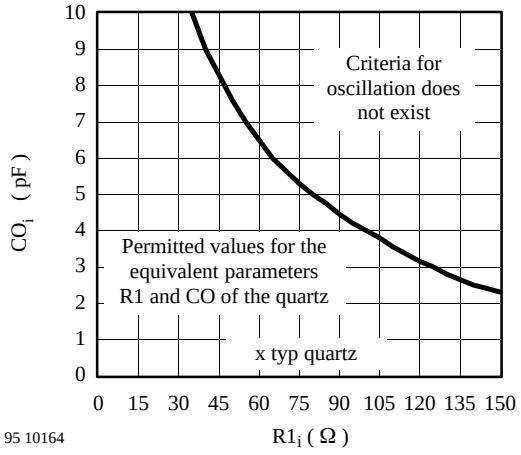


Figure 40. V_{DD} = 2.4 V

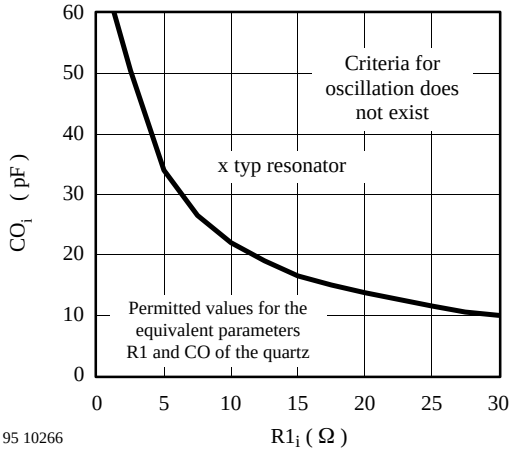


Figure 42. V_{DD} = 2.4 V

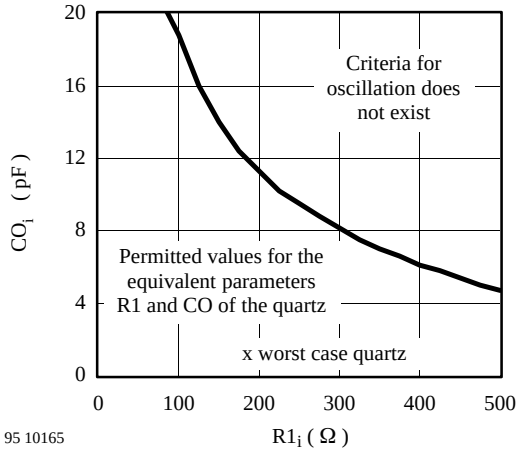


Figure 41. V_{DD} = 3.0 V

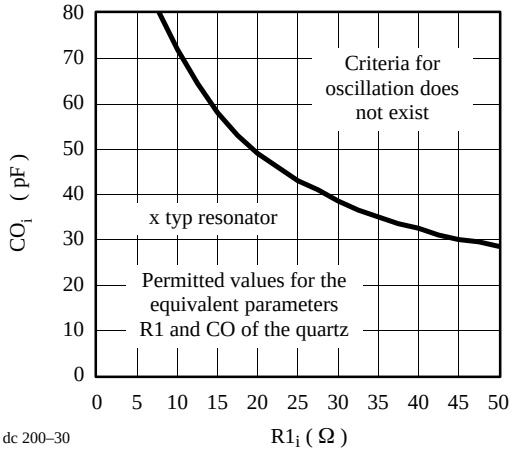


Figure 43. V_{DD} = 3.0 V

Note: For pc-board design place the quartz or ceramic resonator nearby the pins because of low parasitic capacities (≤ 0.5 pF).

6 Characteristics of the Schmitt Trigger Inputs

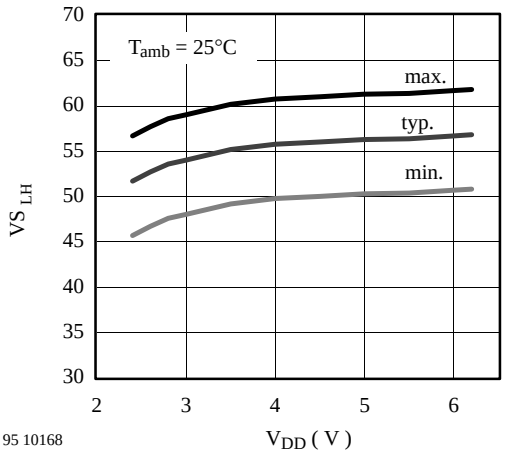


Figure 44. Voltage switch level for positive edge trigger vs. V_{DD}

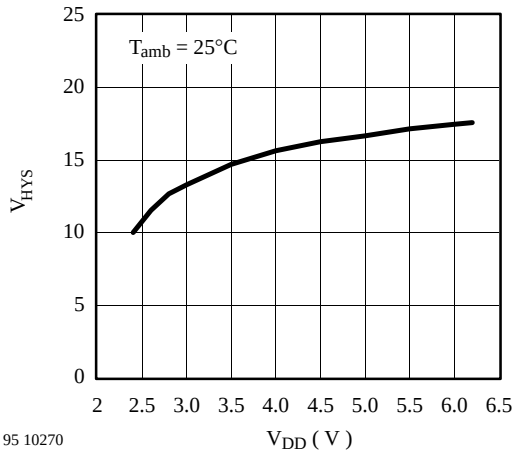


Figure 46. Hystereses in percent of supply voltage vs. V_{DD}

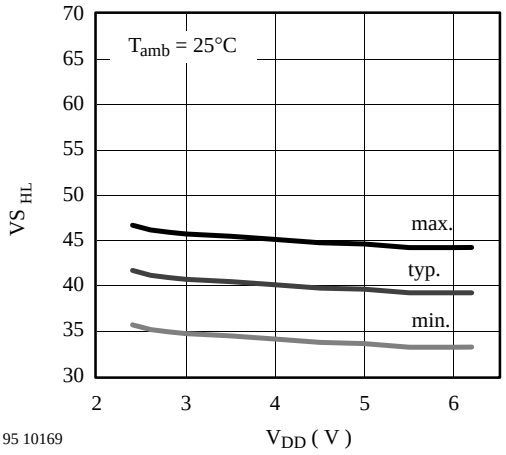


Figure 45. Voltage switch level for negative edge trigger vs. V_{DD}

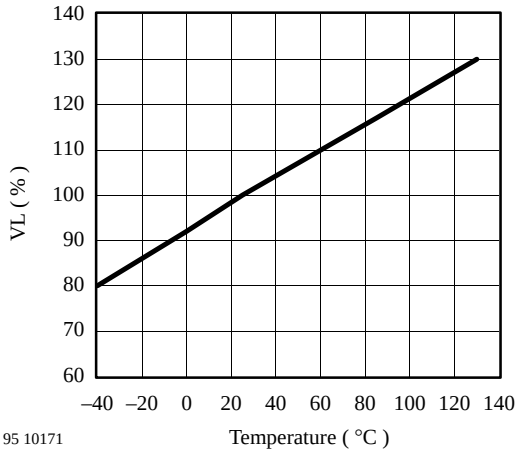


Figure 47. Typical switch level vs. ambient temperature

Note: The values of min., typ. and max. for the positive or negative edge trigger are matched.

Note: For recognize a input pulse a minimum pulse time of 50 ns is necessary. The transition time must be ≤ 10 ns.

7 Ordering Information

Pin options

Please select the option setting from the list below.

Pin	Output		Input	
	CMOS	Open Drain	Pull-Up	Pull-Down
BP00				
BP01				
BP02				
BP03				
BP10				
BP11				
BP12				
BP13				
BP20				
BP21				
BP22				
BP23				
BP30				
BP31				
BP32				
BP33				
IP40–INT6				
IP41–TA				
IP42–TB				
IP43				
NWP				
TE				

ROM code

Please insert ROM CRC.

Size: _____ KByte **CRC:** _____ hex

Approval

Date: _____ Signature: _____

Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC TELEFUNKEN microelectronic GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC TELEFUNKEN microelectronic GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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